REMARKS

In the June 19, 2003, Office Action in this patent application, the United States Patent and Trademark Office (hereinafter "the Office") withdrew Claims 6-15 and 32-41 from consideration, and considered Claims 1-5, 16-31, and 42.

Claims 16-20, 22, and 24 were rejected under 35 U.S.C. § 101 for claiming the same invention as that of Claims 1, 3-6, and 8 of U.S. Patent Application No. 10/167,671, filed June 10, 2002. Claims 25-28, 30, and 42 were rejected under 35 U.S.C. § 103(a) as being unpatentable in view of the teachings of U.S. Patent No. 4,835,479, issued to Haines (hereinafter "Haines"), taken in view of the teachings of U.S. Patent Application No. 2002/0006022, filed by DiSalvo et al. (hereinafter "DiSalvo et al."). Claims 1-5, 16, 22, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable in view of the teachings of U.S. Patent No. 5,083,086, issued to Steiner (hereinafter "Steiner"). Claims 21 and 23 were summarily objected to, but no basis for the objection was explained by the Office.

Applicant appreciates the allowability of Claims 29 and 31, and as suggested by the Examiner, these claim have now been rewritten in independent form to include limitations of the base claims and intervening claims.

To establish *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art as indicated by M.P.E.P. § 2143.03. The cited and applied references do not teach, on the one hand, the concept of charging a capacitance defined between the wire under test and the remaining wires using a current source, or, on the other hand, the concept of calculating the distance to a parallel arcing fault on the wire under test by determining the difference in arrival times among two or more emitted signals, which are produced by a parallel arcing fault as recited in Claims 1, 25, and 42. Moreover, the cited and applied references do not teach the concept of a timing circuit being receptive to the incident waveform and the reflected waveform produced by a parallel arcing fault so as to measure the pulse width of the incident waveform and the reflected waveform and produce a locating signal being proportional to the distance from a device to the parallel arcing fault as recited in Claim 16.

Prior to discussing in detail why applicant believes that all of the claims in this application are allowable, a brief description of applicant's invention and a brief description of the teachings of the cited and applied references are provided. The following background and the discussions of the disclosed embodiments of applicant's invention and the teachings in the cited and applied references are not provided to define the scope or interpretation of any of the claims of this application. Instead, such discussions are provided to help the Office better appreciate important claim distinctions discussed thereafter.

Summary of the Background of the Invention

A parallel arcing fault occurs when an undesired electrical arc bridges the gap between two conductors or a conductor and ground. Developing parallel faults, due to mechanical chafing or aging cracks in the insulation, generally exhibit a progressively declining breakdown voltage until a point is reached where the arcing becomes self-sustaining and dangerous. Such developing faults in the insulation are initially non-conductive and usually so small as to make no perceptible change in the characteristic impedance of the cables. One conventional way to probe such developing faults is to apply a higher-than-normal voltage to the junction (a testing procedure conventionally referred to as HiPot testing). This traditional test, however, allows 10 milliamps of current to flow after breakdown and can heat the insulator sufficiently to form a carbon track and damage the insulation. Moreover, such a test can also damage equipment left connected to the harness during testing. Additionally, wire harnesses in modern forms of transportation, such as an aircraft, are dense, multi-legged, and routed throughout the craft (up to 140 miles of wire in a typical wide-bodied jet). Specific wire bundles may be very long and difficult to access making problematic to locate undesired parallel arcing faults.

Thus, there is a need for a device and method to locate parallel arcing faults without damaging wire insulation or any electronic devices inadvertently connected to the cable harness.

Summary of the Invention

Applicant's invention is directed to locating parallel arc faults without damaging wire insulation or any electronic devices inadvertently connected to a cable harness. More specifically, a device form of the invention includes a device for detecting and locating parallel arcing faults in a set of wires. The voltage at which a parallel arcing fault occurs is below a predetermined test voltage level. Each parallel arcing fault discharges an incident waveform and

a reflected waveform. Each waveform has a pulse width. The device comprises a controller for receiving information and for processing the information to produce a number of control signals. The device further comprises a current source having a first terminal coupled to the controller and a second terminal coupled to a first node. The current source is receptive to a first control signal from the controller at the first terminal to produce direct current at a level as indicated by the first control signal so as to charge a capacitance up to the predetermined testing voltage. The capacitance is defined between a wire under test and the remaining wires of the set of wires. The device yet further comprises a timing circuit having a first terminal coupled to the first node and a second terminal coupled to the controller. The timing circuit is receptive to the incident waveform and the reflected waveform at the first terminal so as to measure the pulse width of the incident waveform and the reflected waveform and produce at the second terminal a locating signal being proportional to the distance from the device to the parallel arcing fault.

One method form of the invention includes a method for detecting parallel arcing faults in a set of wires, the voltage at which a parallel arcing fault occurs is below a predetermined test voltage level. Each parallel arcing fault produces emitted signals that include electromagnetic waveforms and ultrasonic emissions. The method comprises selecting a first wire of the set of wires and defining the first wire as a wire under test while grounding the remaining wires in the set of wires to define these remaining wires as ground wires. The method further comprises charging a capacitance defined between the wire under test and the ground wires using a current source until the voltage on the wire under test ramps up to the predetermined test voltage level. The method yet further comprises calculating the distance to the parallel arcing fault on the wire under test by determining the difference in arrival times among two or more emitted signals.

Another method form of the invention includes a method for detecting parallel arcing faults in a set of wires. Each parallel arcing fault produces two or more electromagnetic waveforms. Each electromagnetic waveform has a leading edge. The method comprises selecting a wire of the set of wires to be defined as the wire under test while coupling the remaining wires in the set of wires to ground. The method further comprises charging a capacitance defined between the wire under test and the remaining wires using a current source. The method yet further comprises finding one of the remaining wires that causes a parallel arcing fault to occur between the wire under test and one of the remaining wires by using a sequencer to

selectively uncouple each wire of the set of wires or couple each wire of the set of wires to the current source or ground.

Another method form of the invention includes a method for detecting parallel arcing faults in a set of wires. The voltage at which a parallel arcing fault occurs is below a predetermined test voltage level. The method comprises selecting a first wire of the set of wires and defining the first wire as a wire under test while grounding the remaining wires in the set of wires to define these remaining wires as ground wires. The method further comprises charging a capacitance defined between the wire under test and the ground wires using a current source until the voltage of the wire under test ramps up to the predetermined test voltage level. The method yet further comprises providing an arc-sensing means responsive to the occurrence of an arc discharge. The method also comprises determining that a parallel arcing fault exists if said arc-sensing means indicates the occurrence of at least one arc discharge.

Summary of Haines

The system of Haines, similar to applicant's invention, is directed to testing cables for current leakage and insulation problems. But, the similarity ends there. As spelled out by the Abstract, Haines describes his invention as follows:

> In order to test the leakage between cores of a multicore cable, a test voltage is applied by a first switch in turn to the cores of a cable whose other end is disconnected. (emphasis provided)

In the system of Haines, before a leakage and insulation test can be performed, a check is performed on the cores of the cable to ensure that no voltages are present. This is accomplished in order to determine whether any potentially harmful voltage is present between each of the cores and ground, and if any voltage is detected which exceeds a preset value corresponding to a reference voltage VR used by the system of Haines. Additionally, the system of Haines checks to see whether any potentially harmful voltages are present between any pair of the cores of the cable. If there is no harmful voltage present between any core and ground or between any pair of cores, a leakage and insulation test may be performed by the system of Haines. Principally, the system of Haines applies a test voltage +V through the cable cores and allows the capacitance between the cores to be charged rapidly via a low-impedance path. Any current leakage is indicated by a volt meter display used by the system of Haines.

Summary of DiSalvo et al.

The system of DiSalvo et al. is directed to a resettable circuit breaker. More specifically, a ground fault circuit interrupting (GFCI) circuit breaker is provided. The circuit breaker has a housing, a circuit interrupting portion, a reset portion, and a reset lockout portion. The housing of the circuit breaker of DiSalvo et al. has line phase and load phase connections that are accessible from an exterior of the housing and a conductive path within the housing between the line and load phase connections. The circuit interrupting portion is disposed within the housing and is configured to open the conductive path upon the occurrence of a ground fault. The reset portion includes an actuator that is also accessible from the exterior of the housing, and is configured to close the conductive path upon actuation.

The system of DiSalvo et al. has a sensing circuitry that includes a path control portion (element 411), a pickup portion (element 412), and a processing portion (element 414). The path control portion provides power to the circuitry used to detect arc faults and to the components used to open the conductive path if an arc fault is detected. The pickup portion monitors the conductive path and picks up spurious signals from the conductive path, which may include arc faults. The processing portion receives the arcing signals and determines whether the arcing signals include an arc fault and provides a trigger signal to open the conductive path if an arc fault is detected. See page 9, paragraph 0102. DiSalvo et al. describes that "[i]t may be desirable for the sensing circuitry to generally pinpoint the location of an arc fault within a branch circuit." See page 12, paragraph 0134. This is accomplished by providing a second arc fault pickup in addition to the original pickup portion so that the pickup portion would output two separate arcing signals representing arcing signals pickup on the line and load sides.

Summary of Steiner

The system of Steiner is directed to locating a fault in electrical conductors from a terminal position which may be remote from the fault using at least a broadband pulse generator to generate a pulse at a terminal position. Steiner also uses a voltage source at the terminal position capable of inducing a change of impedance at the fault; time measuring means also are provided at the terminal position. In an attempt to locate a fault, a method of Steiner involves generating a first pulse at the terminal position, which is propagated down the conductor and reflected back to the terminal position from various impedance discontinuities, including the

impedance discontinuity of the fault, if present. The pattern of reflections from points along the conductor up to the fault resulting from the first pulse are recorded by the method of Steiner. Sufficient voltage is then applied to the cable to induce a change in impedance at the fault. Simultaneously, a method of Steiner generates a second pulse similar to the first pulse at the terminal position and is reflected back from the various impedance discontinuities, including the modified impedance discontinuity at the fault. The reflections of the first pulse are then subtracted from the reflections of the second pulse leaving the pulse reflected from the fault. The location of the fault is then determined from the time taken from the initiation to the reflection of the pulse through the terminal position.

The Claimed Invention Distinguished

The Office has failed to show, and applicant is unable to find, where any of the cited and applied references, either alone or in combination, disclose the subject matter of the claimed invention. The present invention is directed to locating developing parallel arc faults while avoiding or reducing the risk of damaging the wire insulation or electronic devices inadvertently connected to a cable harness. Using Claim 1 as an example, there is no teaching or suggestion in the cited and applied references for locating developing parallel arc faults while avoiding or reducing the risk of damaging the wire insulation or electronic devices inadvertently connected to the cable harness in a manner recited in Claim 1. Claim 1 succinctly defines a method for detecting parallel arcing faults in a set of wires. The method of Claim 1 comprises selecting a first wire of the set of wires and defining the first wire as a wire under test while grounding the remaining wires in the set of wires to define these remaining wires as ground wires. The method further comprises charging a capacitance defined between the wire under test and the ground wires using a current source until the voltage on the wire under test ramps up to the predetermined test voltage level. The method yet further comprises calculating the distance to the parallel arcing fault on the wire under test by determining the difference in arrival times among two or more emitted signals. The cited and applied references do not teach, on the one hand, the concept of using a current source to charge a capacitance defined between the wire under test and the ground wires, and, on the other hand, the concept of calculating the distance to the parallel arcing fault on the wire under test by determining the difference in arrival times among two or more emitted signals.

Like applicant's invention, the system of Steiner is directed to locate a fault in electrical conductors. But the similarity ends there. To understand the differences between the system of Steiner and applicant's claimed invention, it should be noted that the system of Steiner artificially generates a pulse using a pulse generator from a terminal position and causes the pulse to travel down the length of a cable to the fault whereas applicant's claimed invention does not generate a pulse but instead uses a pulse that is naturally caused by a discharge of an arc at the fault. See the preamble of Claim 1 where it is recited that each parallel arcing fault produces emitted signals that include electromagnetic waveforms and ultrasonic emissions. There is no need for applicant's invention to use a pulse generator. On the other hand, the system of Steiner uses a pulse generator to locate a fault.

Another contrast is that the system of Steiner completely lacks a current source as recited in Claim 1. Claim 1 recites that a current source is used to charge a capacitance defined between the wire under test and the ground wires until the voltage on the wire under test ramps up to the predetermined test voltage level. Instead of using a current source, the system of Steiner uses a voltage source at a terminal position. It is respectfully submitted that one skilled in the art recognizes that a voltage source is a circuit element that will maintain a prescribed voltage across its terminals regardless of the current in the device and a current source is a circuit element that will maintain substantially the same current within its terminals regardless of the voltage across its terminals. There is a difference between a voltage source and a current source. Depending on whether a voltage source or a current source is used, the system of Steiner will not work, and the reference Steiner as modified by the Office will be an nonenabling reference.

The Office has likened the pulse generator (element 14) of Steiner as the current source of the claimed invention as recited in Claim 1. This cannot be correct. The current source of the claimed invention is used to charge a capacitance defined between the wire under test and the ground wires until the voltage on the wire under test ramps up to the predetermined test voltage level. The pulse generator of Steiner is used to send an artificial pulse down the length of a cable to locate a fault. It is difficult to understand how the pulse generator of Steiner could be the current source of the claimed invention. Moreover, if Steiner were to use a current source (which he did not), there would be no need for the high-frequency isolation means (element 19 shown in Fig. 1 of Steiner).

In sum, the system of Steiner locates a fault by using a conventional time domain reflectometer method while biasing the fault with a voltage in order to change the fault impedance and thereby cause a reflection to occur. Applicant's claimed invention, in sharp contrast to the system of Steiner, discloses how an edge from a single actual breakdown discharge and its subsequent reflections can be used to measure the distance to the fault. No pulse generator is used by applicant's invention, nor is one needed. The conventional time domain reflectometer method of Steiner applies a short pulse to one end of a transmission line and then looks for reflections that occur at impedance discontinuities. Steiner uses a conventional time domain reflectometer sweep of a transmission line, applies a voltage that modifies the impedance at a fault, and applies a second conventional time domain reflectometer sweep. By comparing the two sweeps, the system of Steiner determines the location of the fault.

The system of Haines, like the system of Steiner, uses a voltage source (element +V coupled to the switch 6 in the sole drawing of Haines). In contrast, applicant's claimed invention recites a current source to charge a capacitance defined between the wire under test and the ground wires so as to locate developing parallel arc faults while avoiding or reducing the risk of damaging the wire insulation or electronic devices inadvertently connected to a cable harness. As discussed above, a current source is a circuit element that will maintain substantially the same current within its terminals regardless of the voltage across its terminals. Thus, a current source is a high-impedance source, which is the opposite of a low-impedance path as required by the system of Haines to charge the capacitance. See Haines at Col. 6, lines 10-14, where Haines discusses that "[t]his allows the capacitance between the cores to be charged rapidly via a low impedance path."

Using Claim 16 as another example, Claim 16 recites a device for detecting and locating parallel arcing faults in a set of wires. The voltage at which a parallel arcing fault occurs is below a predetermined test voltage level. Each parallel arcing fault produces an incident waveform and a reflected waveform. Each waveform has a pulse width. The device comprises a controller for receiving information and for processing the information to produce a number of control signals. The device further comprises a current source having a first terminal coupled to the controller and a second terminal coupled to a first node. The current source is receptive to a first control signal from the controller at the first terminal to produce direct current at a level as indicated by the first control signal so as to charge a capacitance up to the predetermined testing

voltage. The capacitance is defined between a wire under test and the remaining wires of the set of wires. The device yet further comprises a timing circuit having a first terminal coupled to the first node and a second terminal coupled to the controller. The timing circuit is receptive to the incident waveform and the reflected waveform at the first terminal so as to measure the pulse width of the incident waveform and the reflected waveform and produce at the second terminal a locating signal being proportional to the distance from the device to the parallel arcing fault.

As discussed, Steiner lacks a current source. Steiner uses a voltage source. The pulse generator cannot be reasonably interpreted as a current source of the claimed invention. The purpose of the pulse generator is not to charge a capacitance defined between the wire under test and the ground wires but to induce a pulse to sweep a cable line. Steiner also lacks a timing circuit that is receptive to the incident waveform and the reflected waveform at the first terminal so as to measure the pulse width of the incident waveform and the reflected waveform and produce at the second terminal a locating signal being proportional to the distance from the device to the parallel arcing fault. The incident waveform and the reflected waveform are generated naturally from the occurrence of an arc—not artificially generated from a pulse generator.

Steiner or Haines, alone or in combination (whose combination applicant specifically denies), does not disclose the claimed invention. Steiner lacks a current source to charge a capacitance defined between the wire under test and the ground wires. Steiner also induces an artificial pulse by using a pulse generator to sweep a cable. No artificial pulse need be induced by applicant's claimed invention. Unlike Steiner, applicant's claimed invention uses a current source. Haines cannot cure the defects of Steiner because Haines also does not use a current source but instead uses a voltage source. Even if the combination of Steiner and Haines were possible, these references cannot anticipate or render applicant's claimed invention obvious.

As another example, Claims 25 and 42 both recite charging a capacitance defined between the wire under test and the remaining wires using a current source. More generally, Claim 25 succinctly defines a method for detecting parallel arcing faults in a set of wires. Each parallel arcing fault produces two or more electromagnetic waveforms. Each electromagnetic waveform has a leading edge. The method comprises selecting a wire of the set of wires to be defined as the wire under test while coupling the remaining wires in the set of wires to ground.

The method further comprises charging a capacitance defined between the wire under test and the remaining wires using a current source. The method yet further comprises finding one of the remaining wires that causes a parallel arcing fault to occur between the wire under test and one of the remaining wires by using a sequencer to selectively uncouple each wire of the set of wires or couple each wire of the set of wires to the current source or ground. Claim 42 succinctly defines a method for detecting parallel arcing faults in a set of wires, the voltage at which a parallel arcing fault occurs being below a predetermined test voltage level. The method comprises selecting a first wire of the set of wires and defining the first wire as a wire under test while grounding the remaining wires in the set of wires to define these remaining wires as ground wires. The method further comprises charging a capacitance defined between the wire under test and the ground wires using a current source until the voltage of the wire under test ramps up to the predetermined test voltage level. The method yet further comprises providing an arc-sensing means responsive to the occurrence of an arc discharge. The method also comprises determining that a parallel arcing fault exists if said arc-sensing means indicates the occurrence of at least one arc discharge.

Haines does not use a current source but instead uses a voltage source. The Office has indicated that "since both a voltage source and current source are capable of charging a capacitance between conductors, replacing the voltage source with the current source for the purpose of charging a capacitor would be within the level of ordinary skill in the art." Applicant respectfully disagrees. MPEP 2143.01 indicates that "[a] statement that modifications of the prior art to meet the claimed invention would have been 'well within the ordinary skill of the art at the time the claimed invention was made' ... is not sufficient to establish a *prima facie* case of obviousness." Additionally, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *Id.* The problem with Haines is that Haines must use a voltage source, which is coupled to a low impedance path, so as to charge the core quickly. A current source is a high-impedance element and would change the principle operation of Haines.

DiSalvo et al. does not use a current source to charge a capacitance defined between the wire under test and the ground wires. In fact, DiSalvo et al. does not even charge a line for the purpose of testing. Therefore, DiSalvo et al. cannot cure the defects of Haines. There is no

benefit to combining Haines and DiSalvo et al. Even if the combination of Haines and DiSalvo et al. were possible, which applicant specifically denies, the combination would not anticipate or render unpatentable the claimed invention.

The Office indicated that DiSalvo et al. discloses the following:

> DiSalvo et al. disclose [a calculation of a] distance to a parallel arcing fault wherein the distance is calculated by determining the difference in arrival times among two or more emitted signals (Paragraph 134, lines 1-8). Specifically, the method of acquiring the arrival times is implemented by placing one receiver at one terminal [sic] the wire under test and another receiver at the other terminal of the wire under test, and calculating the difference in the arrival time of one leading edge receive [sic] at the one receiver and the arrival time of the other leading edge received at the other receiver (Paragraphs 134-137).

It is difficult to understand what this has to do with Claims 25 and 42 since the language of Claims 25 and 42 does not require such features. But even if somehow such disclosure is relevant, a reading of the cited portions of DiSalvo et al. at paragraphs 134-137 does not seem to match what the Office has indicated as being disclosed by DiSalvo et al. DiSalvo et al. describes that "[i]t may be desirable for the sensing circuitry to generally pinpoint the location of an arc fault within a branch circuit." See page 12, paragraph 0134. While this might sound promising, what DiSalvo et al. actually pinpoints is whether an arc occurs on a line side or on a load side of the circuit of DiSalvo et al. This is accomplished by providing a second arc fault pickup in addition to the original pickup portion so that the pickup portion would output two separate arcing signals representing arcing signals pickup on the line and load sides.

All that applicant can find in paragraphs 134-137 of DiSalvo et al. is that by using two arc sensing circuits (one on the line side, which is the input to the breaker, and one on the load side, which is the output from the breaker), a determination can be made of whether the arc originates on the line side or the load side. In other words, if the detected noise amplitude is higher on the line side then the arc probably originates somewhere on the line side of the circuit breaker and on the load side if otherwise. For this to work, the impedance of the breaker itself must be relatively large at high frequencies so as to attenuate the high frequencies that pass

through it and prevent both detectors from responding the same way. As DiSalvo et al. states in paragraph 135: "Referring to FIG. 27, the line and load arc fault pickups are, preferably, separated by the transformer assemblies 570 and 572 and ferrite transformers or beads 604 and 606 and located on each side of the transformer assemblies. The ferrite transformers function to enhance the impedance of the AC line to high frequency signals." The purpose for these beads is to isolate the two arc fault "pickups" from each other. DiSalvo et al. has no capability to locate precisely where on the power line an arc occurs.

Because the Office has failed to state a prima facie case of obviousness, the rejection should be withdrawn. Independent Claims 1, 16, 25, and 42 are clearly patentably distinguishable over the cited and applied references. Claims 2-5 and 17-31 are allowable because they depend from allowable independent claims and because of the additional limitations added by those claims. Consequently, reconsideration and allowance of Claims 1-5, 16-31, and 42 is respectfully requested.

Double Patenting

Applicant respectfully submits that the Office has incorrectly rejected Claims 16-20, 22, and 24 of the pending patent application as being in conflict with Claims 1, and 3-6 of U.S. Patent Application No. 10/167,671, under 35 U.S.C. 101. In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is whether the same invention is being claimed twice. The term "same invention" means identical subject matter. See MPEP Section 804, citing *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1984); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA); and *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).

The subject matter of Claims 16-20, 22, and 24 of the pending patent application is not identical to the subject matter of Claims 1, and 3-6 of U.S. Patent Application No. 10/167,671. Thus, there cannot be a conflict. Given that the double patenting rejection is in error, withdrawal of the rejection and allowance of these claims is respectfully requested.

CONCLUSION

In view of the foregoing remarks, applicant submits that all of the claims in the present invention, as amended, are clearly patentably distinguishable over the teachings of Haines, DiSalvo et al., and Steiner, taken alone or in combination. Thus, applicant submits that this application is in condition for allowance. Reconsideration and reexamination of the application, allowance of the claims, and passing of the application to issue at an early date are solicited. If the Examiner has any remaining questions concerning this application, the Examiner is invited to contact the applicant's undersigned attorney at the number below.

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The Commissioner is hereby authorized to charge any additional fees that may be due, including extension fees, or credit any overpayment to our Deposit Account No. 08-3038 (Order No. 03015.0003.NPUS01).

Respectfully submitted,

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